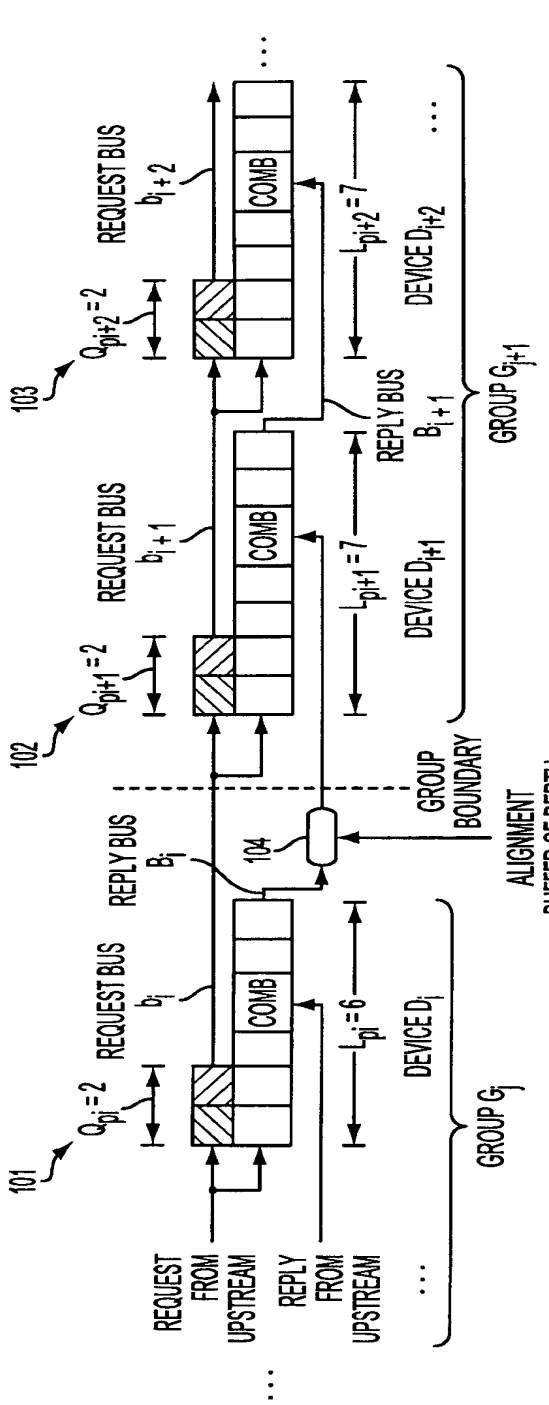
101
102
103
104
REQUEST FROM UPSTREAM
REPLY FROM UPSTREAM
REQUEST BUS
REPLY BUS
COMB
DEVICE D_i
DEVICE D_{i+1}
DEVICE D_{i+2}
GROUP G_j
GROUP G_{j+1}
GROUP BOUNDARY
ALIGNMENT BUFFER OF DEPTH $L_{pi+1} - L_{pi} = 1$
$Q_{pi} = 2$
$Q_{pi+1} = 2$
$Q_{pi+2} = 2$
$L_{pi} = 6$
$L_{pi+1} = 7$
$L_{pi+2} = 7$
b_i
b_{i+1}
b_{i+2}
B_i
B_{i+1}

FIG. 1

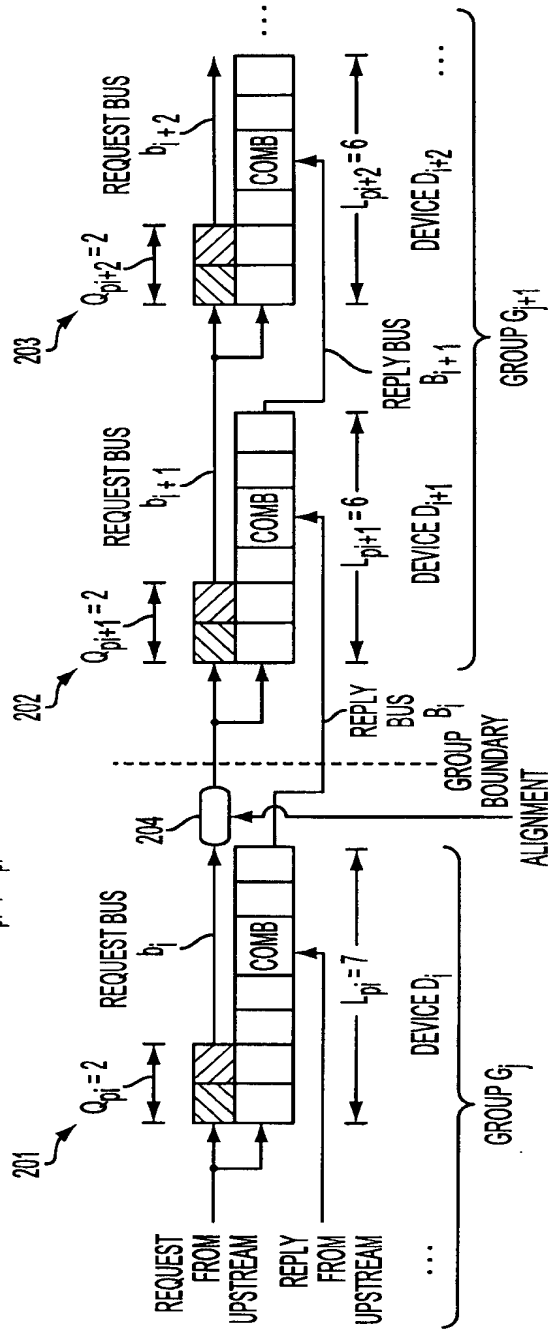
201
202
203
204
REQUEST FROM UPSTREAM
REPLY FROM UPSTREAM
REQUEST BUS
REPLY BUS
COMB
DEVICE D_i
DEVICE D_{i+1}
DEVICE D_{i+2}
GROUP G_j
GROUP G_{j+1}
GROUP BOUNDARY
ALIGNMENT BUFFER OF DEPTH $L_{pi} - L_{pi+1} = 1$
$Q_{pi} = 2$
$Q_{pi+1} = 2$
$Q_{pi+2} = 2$
$L_{pi} = 7$
$L_{pi+1} = 6$
$L_{pi+2} = 6$
b_i
b_{i+1}
b_{i+2}
B_i
B_{i+1}

FIG. 2

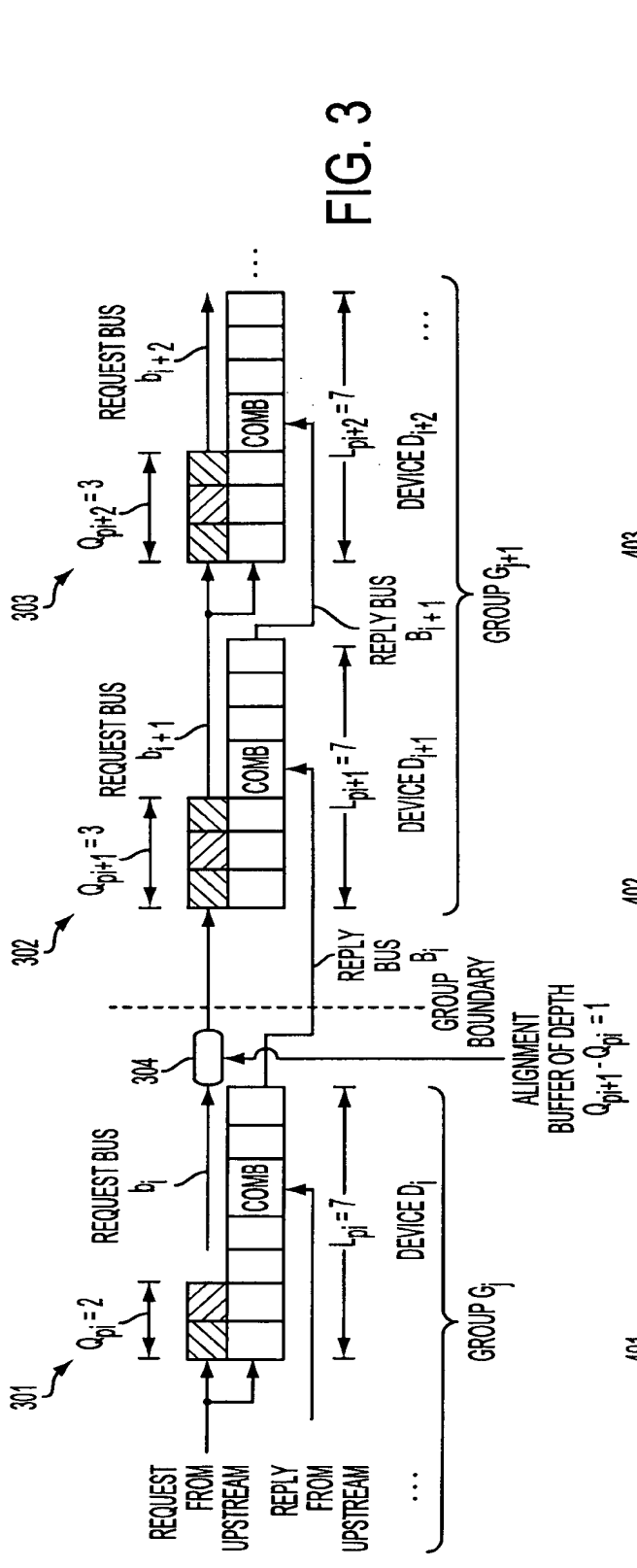
301
302
303
304
REQUEST FROM UPSTREAM
REPLY FROM UPSTREAM
REQUEST BUS
REPLY BUS
COMB
DEVICE D_j
DEVICE D_{j+1}
DEVICE D_{j+2}
GROUP G_j
GROUP G_{j+1}
GROUP BOUNDARY
ALIGNMENT BUFFER OF DEPTH $Q_{pi+1} - Q_{pi} = 1$

FIG. 3

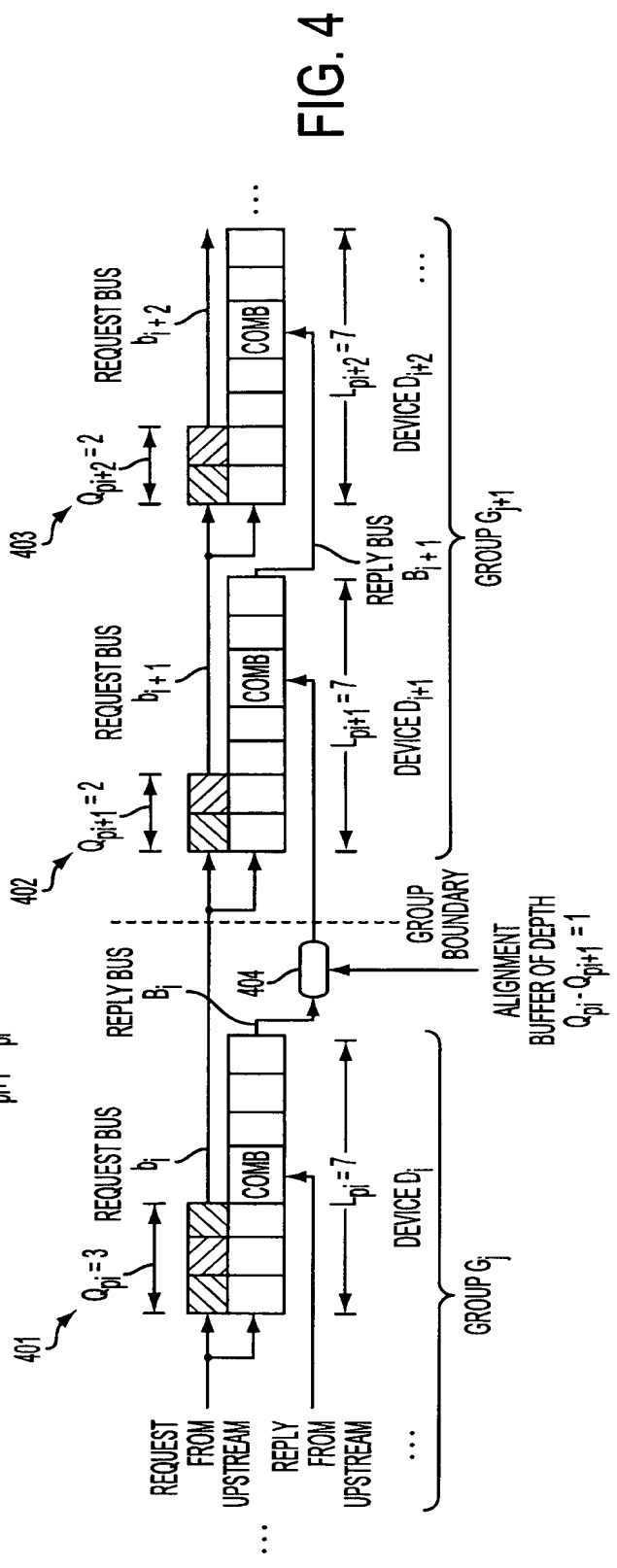
401
402
403
404
REQUEST FROM UPSTREAM
REPLY FROM UPSTREAM
REQUEST BUS
REPLY BUS
COMB
DEVICE D_j
DEVICE D_{j+1}
DEVICE D_{j+2}
GROUP G_j
GROUP G_{j+1}
GROUP BOUNDARY
ALIGNMENT BUFFER OF DEPTH $Q_{pi} - Q_{pi+1} = 1$

FIG. 4

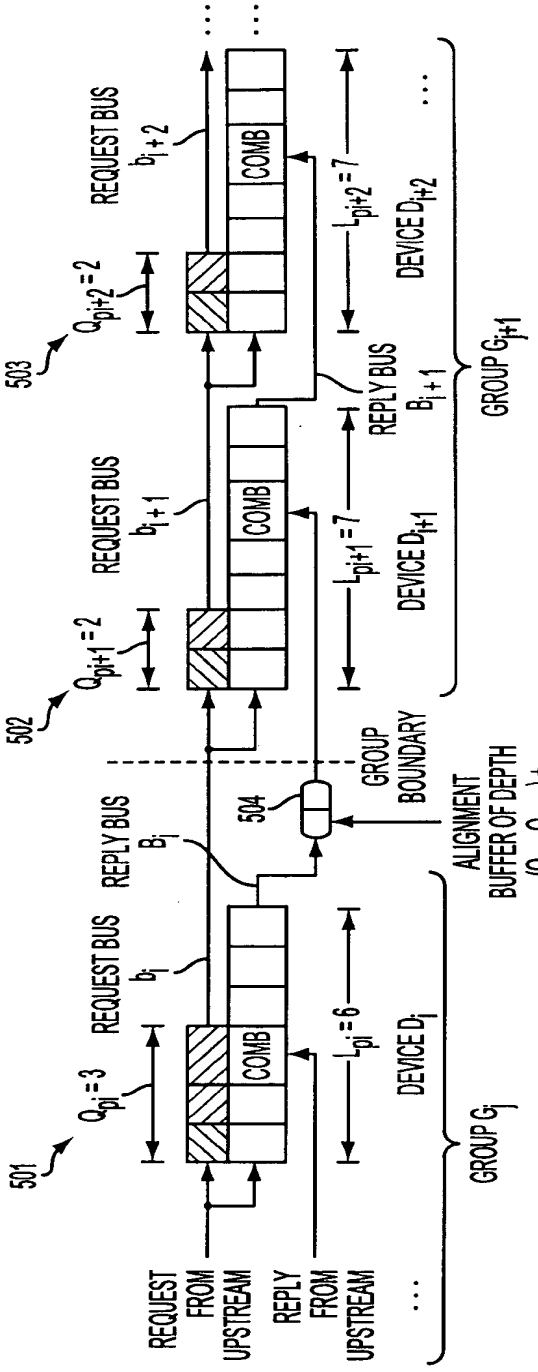
REQUEST FROM UPSTREAM
REPLY FROM UPSTREAM
501
502
503
504
REQUEST BUS
REPLY BUS
COMB
GROUP BOUNDARY
ALIGNMENT BUFFER OF DEPTH
DEVICE
GROUP

FIG. 5

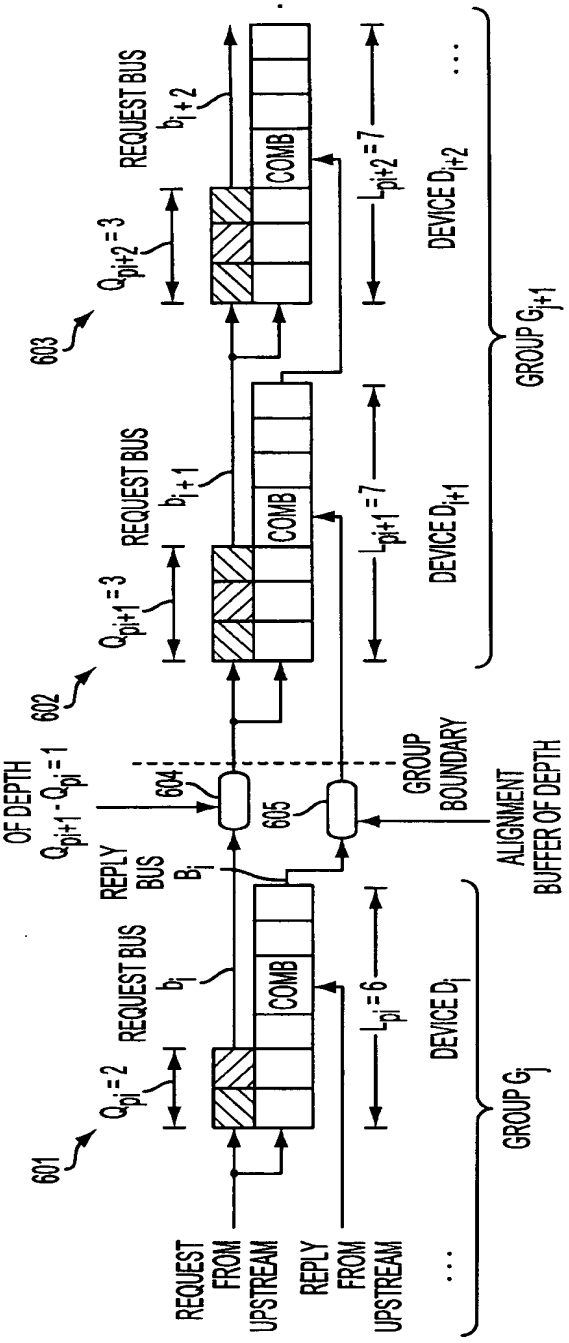
REQUEST FROM UPSTREAM
REPLY FROM UPSTREAM
601
602
603
604
605
REQUEST BUS
REPLY BUS
COMB
GROUP BOUNDARY
ALIGNMENT BUFFER OF DEPTH
DEVICE
GROUP

FIG. 6

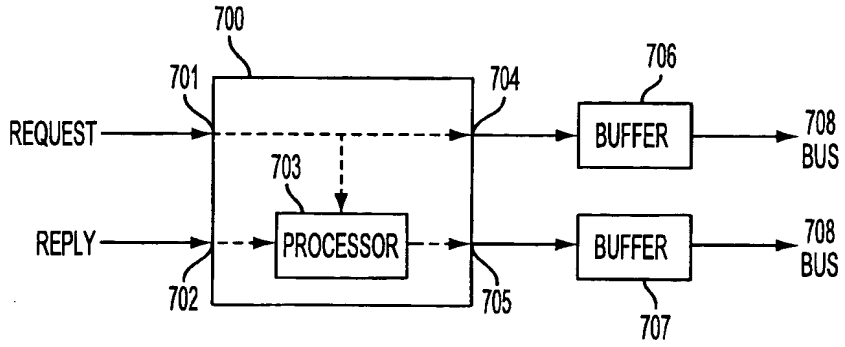

FIG. 7a

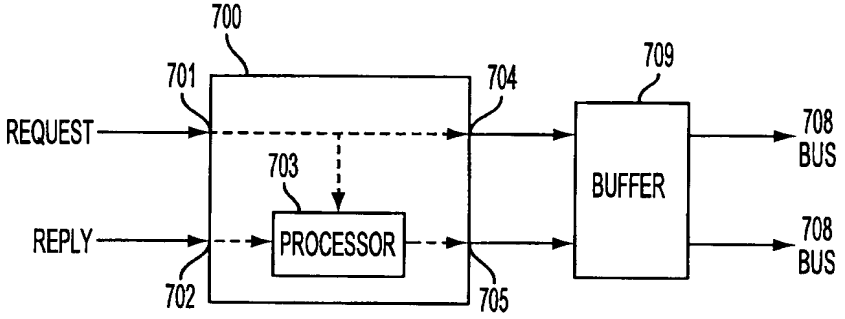

FIG. 7b

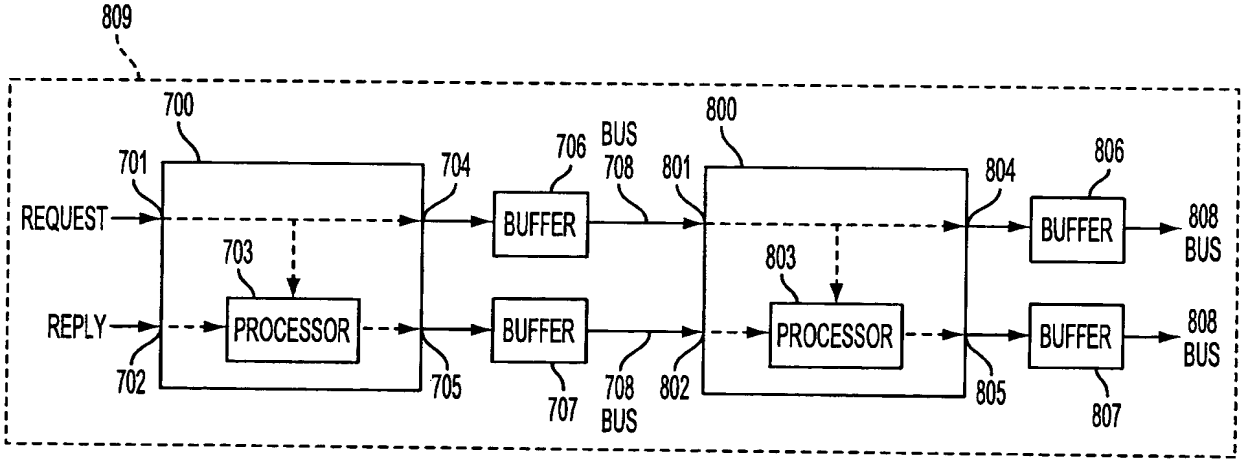

FIG. 8

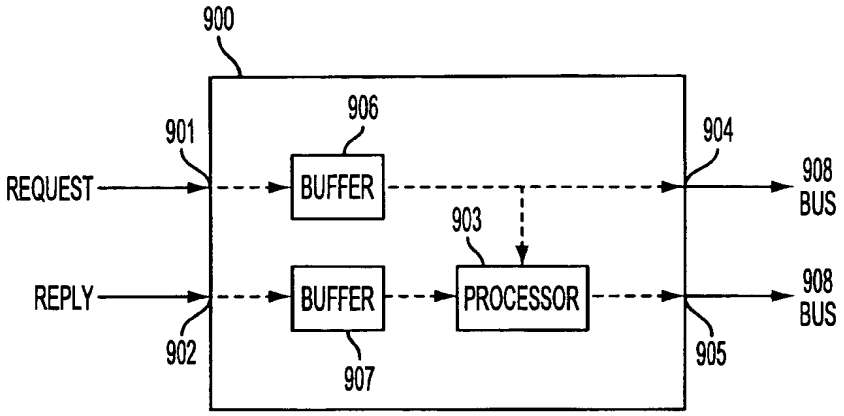
900
906
901
904
REQUEST
BUFFER
908
BUS
903
REPLY
BUFFER
PROCESSOR
908
BUS
902
907
905

FIG. 9

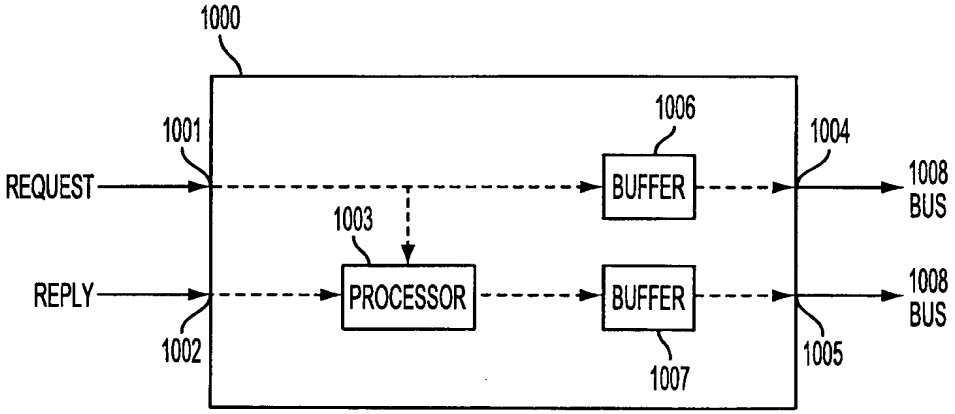
1000
1006
1001
1004
REQUEST
BUFFER
1008
BUS
1003
REPLY
PROCESSOR
BUFFER
1008
BUS
1002
1007
1005

FIG. 10

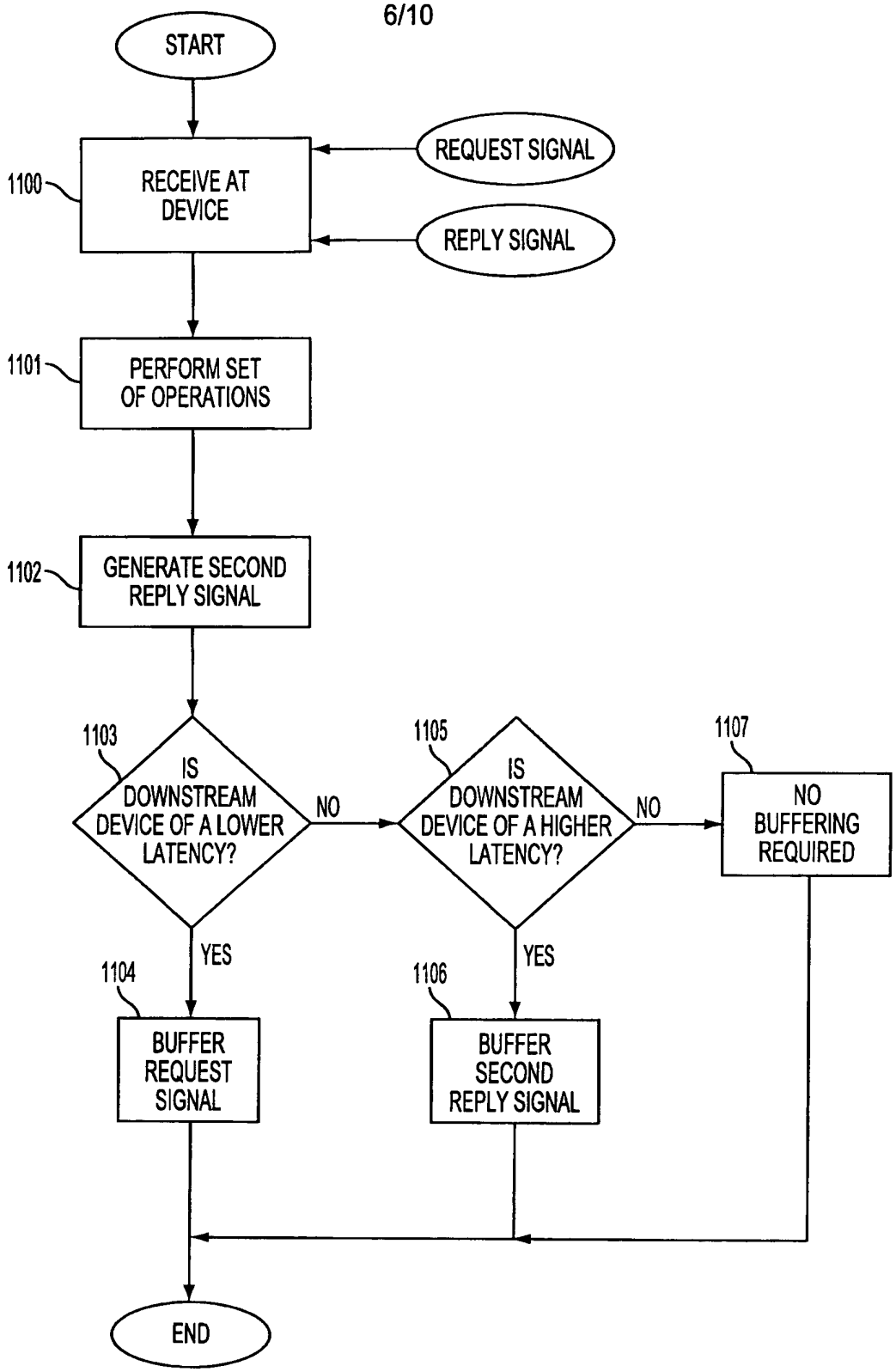
START
REQUEST SIGNAL
REPLY SIGNAL
1100
RECEIVE AT DEVICE
1101
PERFORM SET OF OPERATIONS
1102
GENERATE SECOND REPLY SIGNAL
1103
IS DOWNSTREAM DEVICE OF A LOWER LATENCY?
NO
1105
IS DOWNSTREAM DEVICE OF A HIGHER LATENCY?
NO
1107
NO BUFFERING REQUIRED
YES
1104
BUFFER REQUEST SIGNAL
YES
1106
BUFFER SECOND REPLY SIGNAL
END

FIG. 11

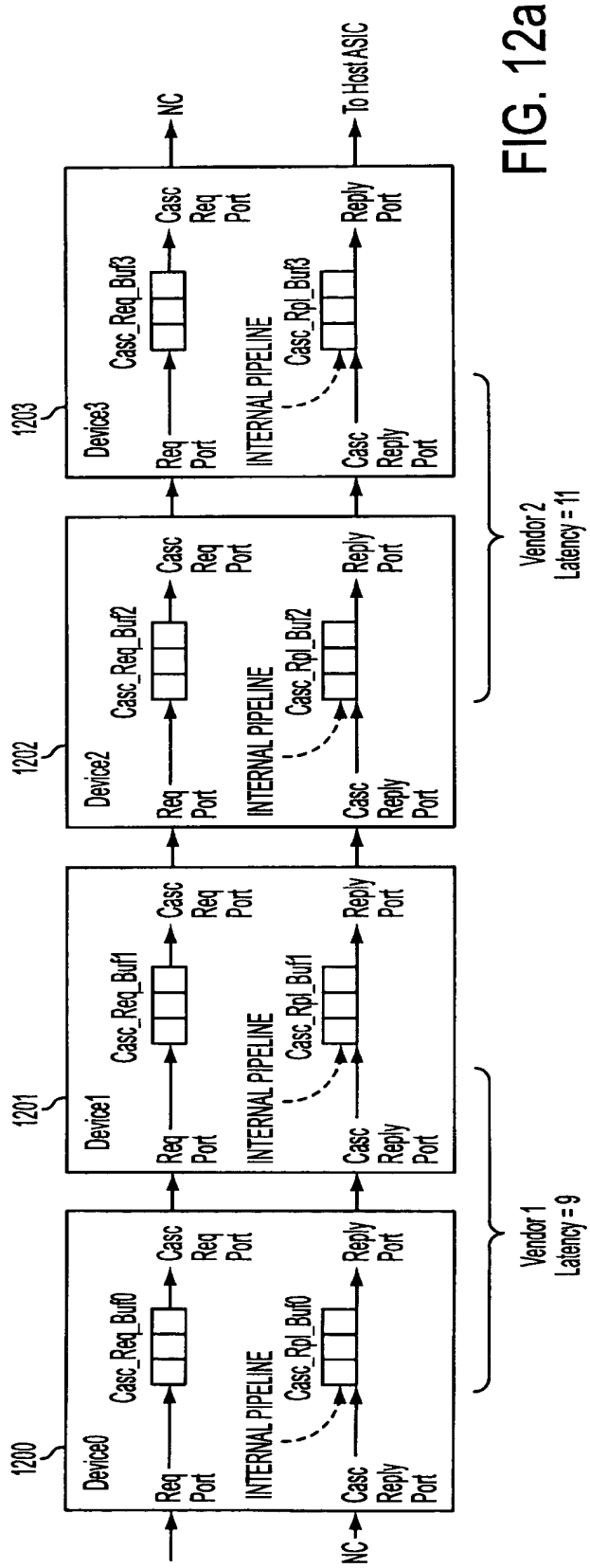

FIG. 12a

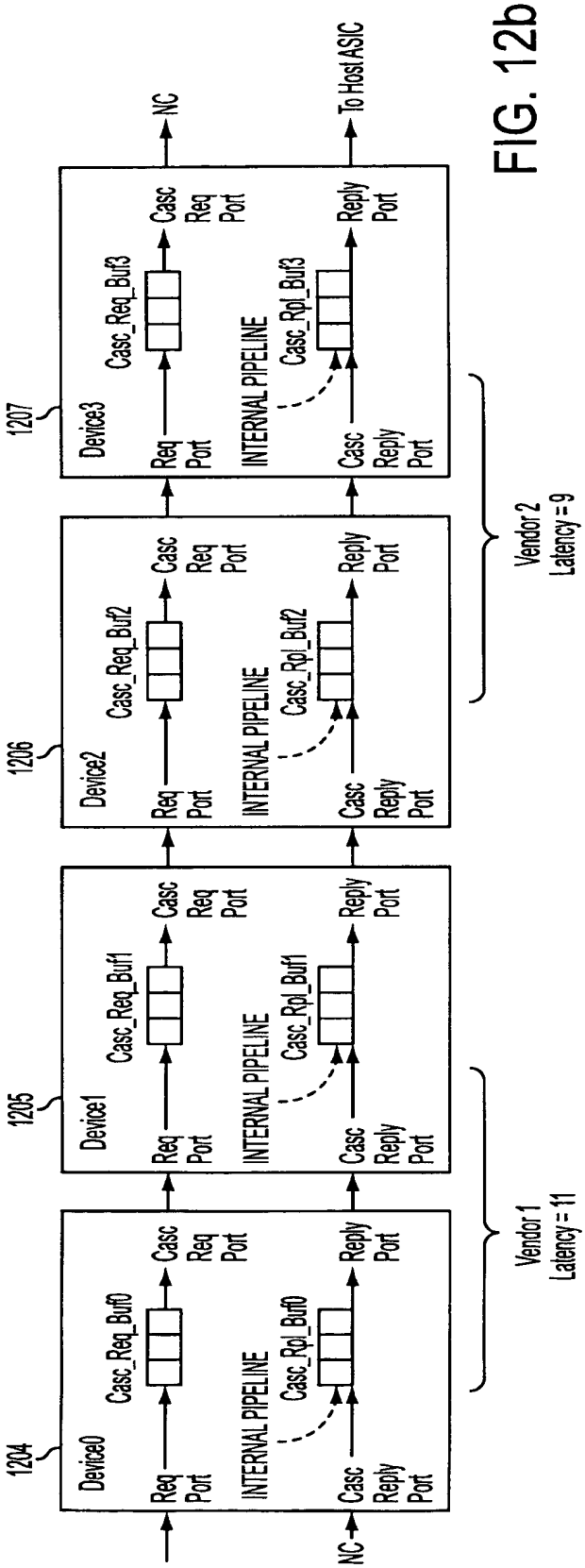

FIG. 12b

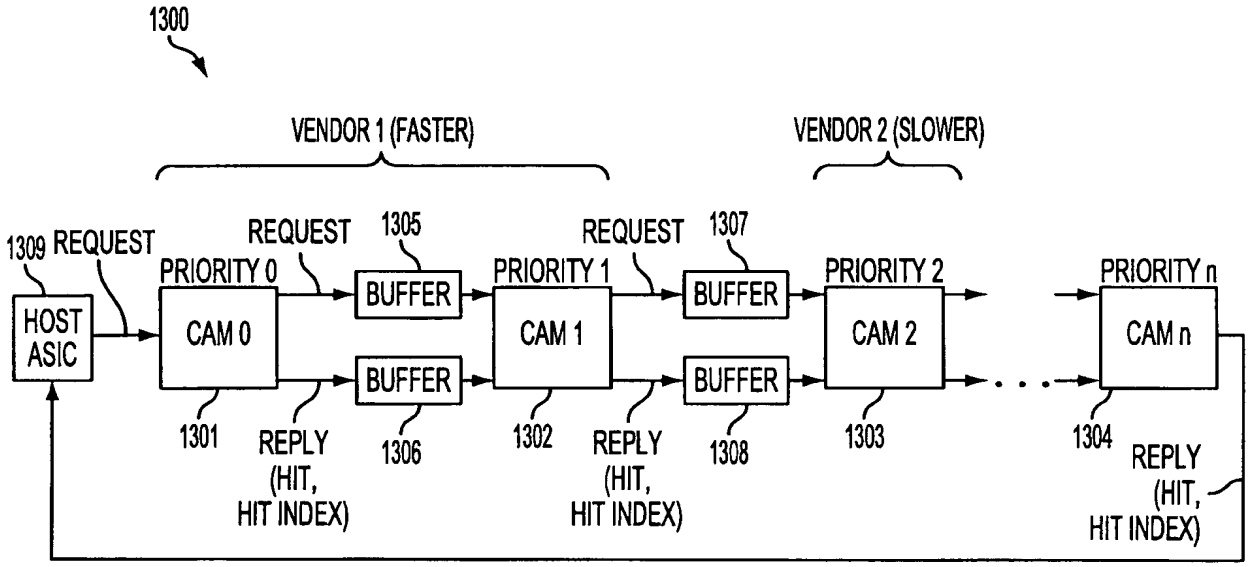
1300
VENDOR 1 (FASTER)
VENDOR 2 (SLOWER)
1309
REQUEST
REQUEST
1305
REQUEST
1307
PRIORITY 0
PRIORITY 1
PRIORITY 2
PRIORITY n
HOST ASIC
CAM 0
BUFFER
CAM 1
BUFFER
CAM 2
CAM n
BUFFER
BUFFER
1301
REPLY (HIT, HIT INDEX)
1306
1302
REPLY (HIT, HIT INDEX)
1308
1303
1304
REPLY (HIT, HIT INDEX)

FIG. 13

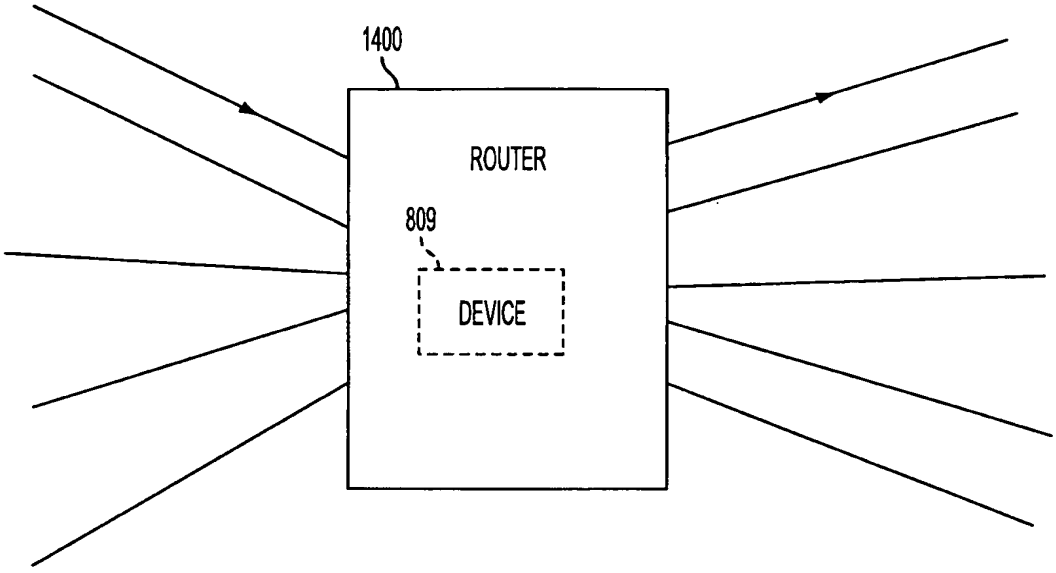

FIG. 14

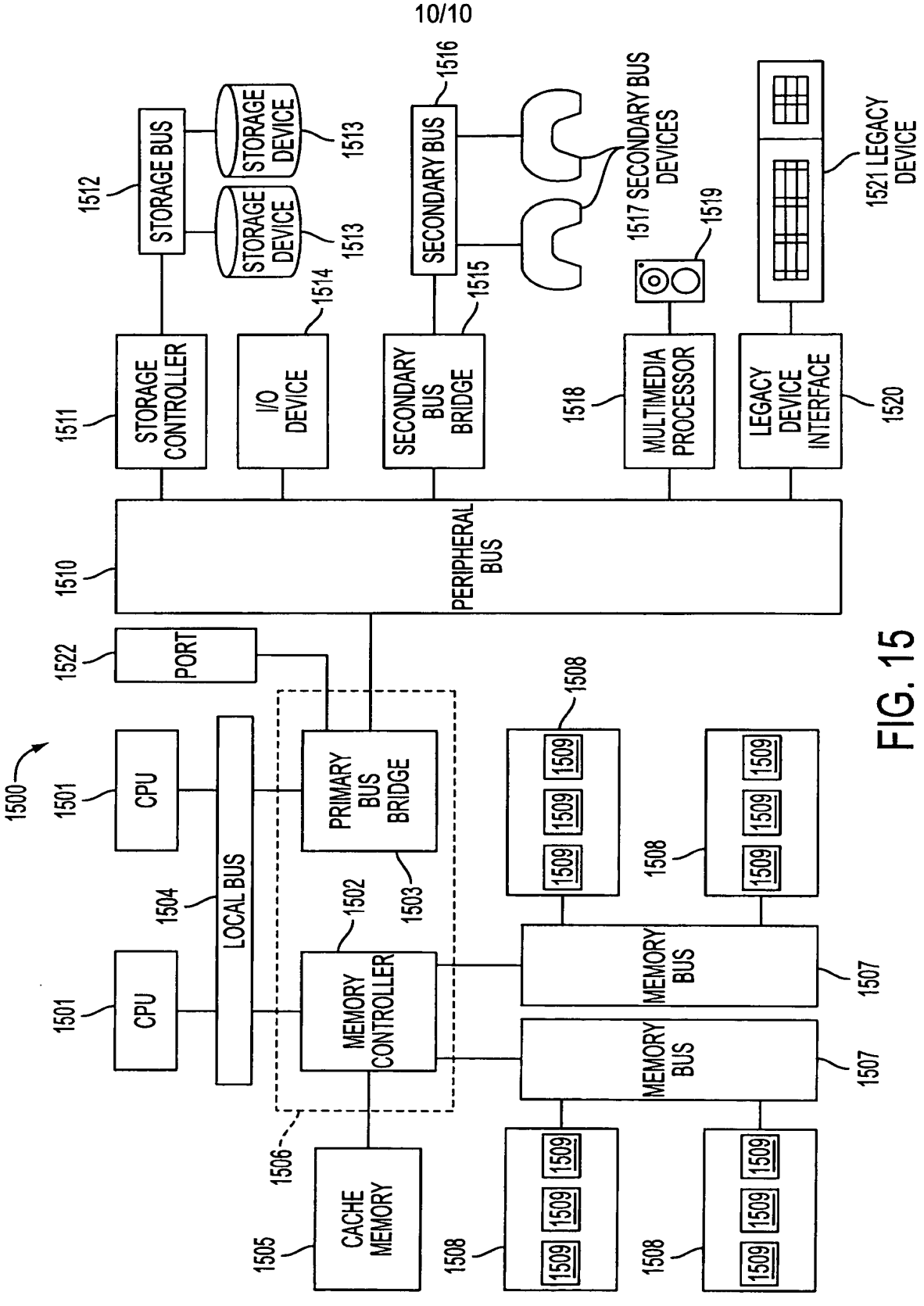
1500
1501
CPU
1501
CPU
1504
LOCAL BUS
1502
MEMORY CONTROLLER
1503
PRIMARY BUS BRIDGE
1506
CACHE MEMORY
1505
1522
PORT
1510
PERIPHERAL BUS
1511
STORAGE CONTROLLER
1512
STORAGE BUS
STORAGE DEVICE
1513
STORAGE DEVICE
1513
1514
I/O DEVICE
1515
SECONDARY BUS BRIDGE
1516
SECONDARY BUS
1517 SECONDARY BUS DEVICES
1518
MULTIMEDIA PROCESSOR
1519
1520
LEGACY DEVICE INTERFACE
1521 LEGACY DEVICE
1507
MEMORY BUS
1507
MEMORY BUS
1508
1509
1508
1509
1508
1509
1508
1509

FIG. 15